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FAIRCHILD SEMICONDUCTOR TM

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ML2036

Serial Input Programmable Sine Wave Generator with Digital Gain Control

Features

- Programmable output frequency – DC to 50kHz
- Low gain error and total harmonic distortion
- 3-wire SPI compatible serial microprocessor interface with double buffered data latch
- Fully integrated solution – no external components required
- Frequency resolution of 1.5Hz (±0.75Hz) with a 12MHz clock input
- Onboard 3 to 12MHz crystal oscillator
- Clock outputs of 1/2 or 1/8 of the input clock frequency
- Synchronous or asynchronous data loading capability
- Compatible with ML2004 logarithmic gain/attenuator

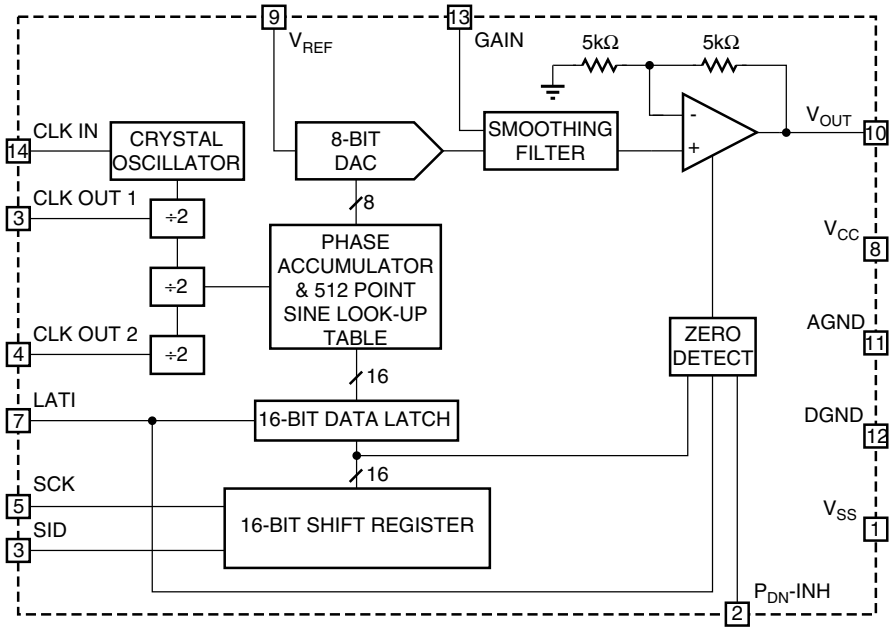
General Description

The ML2036 is a monolithic sine wave generator whose output is programmable from DC to 50kHz. No external components are required. The frequency of the sinewave output is derived from either an external crystal or clock input, providing a stable and accurate frequency reference. The frequency is programmed by a 16-bit serial data word.

The ML2036 provides for a V_{OUT} amplitude of either $\pm V_{REF}$ or $\pm V_{REF}/2$. Also included with the ML2036 is an inhibit function which allows the sinewave output to be held at zero volts after completing the last half cycle of the sine wave in progress. Two digital clock outputs are provided to drive other devices with one half or one eighth of the input clock frequency.

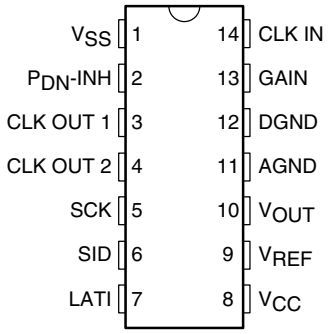
The ML2036 is intended for telecommunications and modem applications that need low cost and accurate generation of precise test tones, call progress tones, and signaling tones.

Block Diagram (Pin configuration shown for 14-Pin PDIP Version)



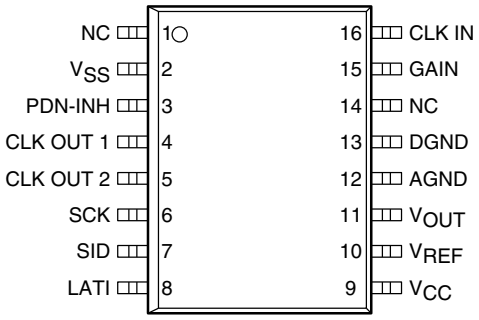
Pin Configuration

ML2036
14-Pin PDIP (P14)



TOP VIEW

ML2036
16-Pin Wide SOIC (S16W)



TOP VIEW

Pin Description (Pin Number in Paranthesis is for SOIC Version)

PIN	NAME	FUNCTION
1 (2)	V_{SS}	Negative supply (-5V).
2 (3)	P_{DN}-INH	Three level input which controls the inhibit and power down modes. Current source pull-up to V_{CC}.
3 (4)	CLK OUT 1	Digital clock output from the internal clock generator that can drive other devices at $f_{CLK\ OUT\ 1} = f_{CLK\ IN}/2$.
4 (5)	CLK OUT 2	Digital clock output from the internal clock generator that can drive other devices at $f_{CLK\ OUT\ 2} = f_{CLK\ IN}/8$.
5 (6)	SCK	Serial clock. Digital input which clocks in serial data on its rising edges.
6 (7)	SID	Serial input data which programs the frequency of V_{OUT}.
7 (8)	LATI	Digital input which latches serial data into the internal data latch on falling edges.
8 (9)	V_{CC}	Positive supply (5V).
9 (10)	V_{REF}	Reference input. The voltage on this pin determines the peak-to-peak swing of V_{OUT}. V_{REF} can be tied to V_{CC}.
10 (11)	V_{OUT}	Analog output.
11 (12)	AGND	Analog ground. All analog inputs and outputs are referenced to this point.
12 (13)	DGND	Digital ground. All digital inputs and outputs are referenced to this point.
13 (15)	GAIN	Sets V_{OUT} peak amplitude to V_{REF} or $V_{REF}/2$. Current source pull-down to DGND.
14 (16)	CLK IN	Clock input. The internal clock can be generated by tying a 3 to 12MHz crystal from this pin to DGND, or by applying a digital clock signal directly to the pin.

Absolute Maximum Ratings

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Parameter	Min.	Max.	Units
V_{CC}		6.5	V
V_{SS}		-6.5	V
V_{OUT}	V_{SS} - 0.3	V_{CC} + 0.3	V
Voltage on any other pin	GND - 0.3	V_{CC} + 0.3	V
Input Current		±25	mA
Junction Temperature		150	°C
Storage Temperature Range	–65	150	°C
Lead Temperature (Soldering, 10 sec)		260	°C
Thermal Resistance (θ_{JA}) 14-Pin PDIP 16-Pin Wide SOIC		 88 105	 °C/W °C/W

Operating Conditions

Parameter	Min.	Max.	Units
Temperature Range ML2036CX ML2036IX	 0 -40	 70 85	 °C °C
V_{CC} Range	4.5	5.5	V
V_{SS} Range	-4.5	-5.5	V

Electrical Characteristics

Unless otherwise specified, V_{CC} = 4.5V to 5.5V, V_{SS} = -4.5V to -5.5V, V_{REF} = 2.5V to V_{CC}, CLK IN = 12.352MHz, C_L = 100pF, R_L = 1kΩ, T_A = Operating Temperature Range (Note 1)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
Output							
HD	Harmonic Distortion (Note 2) (2nd and 3rd Harmonic)	20Hz to 5kHz				-45	dB
		5kHz to 50kHz				-40	dB
SND	Signal to Noise + Distortion (Note 2)	200Hz to 3.4kHz, f_{OUT}BW = 200Hz to 4kHz				-45	dB
		20Hz to 50kHz, f_{OUT} BW = 20 Hz to 150kHz				-40	dB
V_{GN}	Gain Error (Note 2)	20Hz < f_{OUT} < 5kHz				±0.15	dB
		5kHz < f_{OUT} < 50kHz				±0.3	dB
ICN	Idle Channel Noise	Power Down Mode, Cmsg Weighted			-20	0	dBrnc
		Power Down Mode, 1kHz			50		nV/√Hz
		Inhibit Mode, 1kHz			500		nV/√Hz
PSRR	Power Supply Rejection Ratio	200mV_{P-P}, 0 - 10kHz Sine, Measured on V_{OUT}	V_{CC}			-40	dB
			V_{SS}			-40	dB
V_{OS}	V_{OUT} Offset Voltage (Note 3)					±(2.5+ V_{P-P})/100	V
V_{P-P}	Peak-to-Peak Output Voltage (Note 2)	GAIN = V_{CC}			±V_{REF}		V
		GAIN = DGND			±V_{REF}/2		V
	V_{OUT} Swing	GAIN = V_{CC}		V_{SS} +1.5		V_{CC} -1.5	V
R_{REF}	Reference Input Resistance			1	6		MΩ

Electrical Characteristics (continued)

Unless otherwise specified, V_{CC} = 4.5V to 5.5V, V_{SS} = -4.5V to -5.5V, V_{REF} = 2.5V to V_{CC}, CLK IN = 12.352MHz, C_L = 100pF, R_L = 1kΩ, T_A = Operating Temperature Range (Note 1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Oscillator						
V_{IL} CLK	CLK IN Input Low Voltage				1.5	V
V_{IH} CLK	CLK IN Input High Voltage		3.5			V
I_{IL} CLK	CLK IN Input Low Current		-250			µA
I_{IH} CLK	CLK IN Input High Current				250	µA
C_{IN} CLK	CLK IN Input Capacitance			12		pF
t_{CKI}	CLK IN On/Off Period	t_R = t_F = 10ns, 2.5V Midpoint	30			ns
	CLK OUT 1/CLK IN Frequency Ratio	See Figure 2	0.49		0.51	
	CLK OUT 2/CLK IN Frequency Ratio	See Figure 2	0.122		0.128	
t_{1R}, t_{2R}	CLK OUT 1, CLK OUT 2 Rise Time	C_L = 40pF, 10% to 90%			20	ns
		C_L = 100pF, 0.8V to 2.0V Transition			20	ns
t_{1F}, t_{2F}	CLK OUT 1, CLK OUT 2 Fall Time	C_L = 40pF, 90% to 10%			20	ns
		C_L = 100pF, 2.0V to 0.8V Transition			20	ns
Logic						
V_{IL}	Input Low Voltage (LATI, SCK, SID, GAIN)				0.8	V
V_{IH}	Input High Voltage (LATI, SCK, SID, GAIN)		2.0			V
V_{I1}	Input Low Voltage - P_{DN}-INH		-0.5		0.8	V
V_{I2}	Inhibit Stage Voltage - P_{DN}-INH				V_{SS} + 0.5	V
V_{I3}	Input High Voltage - P_{DN}-INH		2.0			V
I_{IL}-P_{DN}	P_{DN}-INH Input Low Current	P_{DN}-INH = 0V	-70	-20	-5	µA
I_{IH}-GAIN	GAIN Input High Current	GAIN = V_{CC}	5	20	70	µA
I_{IL}	Input Low Current (LATI, SCK, SID, GAIN)	V_{IN} = 0V	-1			µA
I_{IH}	Input High Current (LATI, SCK, SID, GAIN)	V_{IN} = V_{CC}			1	µA
C_{IN}	Input Capacitance			5		pF
V_{OL}	Output Low Voltage	I_{OL} = -2mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = 2mA	4.0			V
t_{SCK}	Serial Clock On/Off Period		100			ns
t_{DS}	SID Data Setup Time		50			ns
t_{DH}	SID Data Hold Time		50			ns
t_{LPW}	LATI Pulse Width		50			ns
t_{LH}	LATI Hold Time		50			ns
t_{LS}	LATI Setup Time		50			ns
Supply						
I_{CC}	V_{CC} Current	No Load, V_{CC} = V_{REF} = 5.5V			5.5	mA
		No Load, Power Down Mode			2	mA
I_{SS}	V_{SS} Current	No Load, V_{CC} = V_{REF} = 5.5V, V_{SS} = -5.5V			-3.5	mA
		No Load, Power Down Mode			-100	µA

Notes:

1. Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.
2. Maximum peak-to-peak voltage for the output sine wave is: $V_{OUT(P-P)} \leq$ (125kV x Hz)/f_{OUT}. For example, at 50kHz, the maximum output voltage swing is 2.5V_{P-P}.
3. Offset voltage is a function of the peak-to-peak output voltage. For example, if $V_{OUT(P-P)}$ = 2.5V, V_{OS}= ±50mV max.

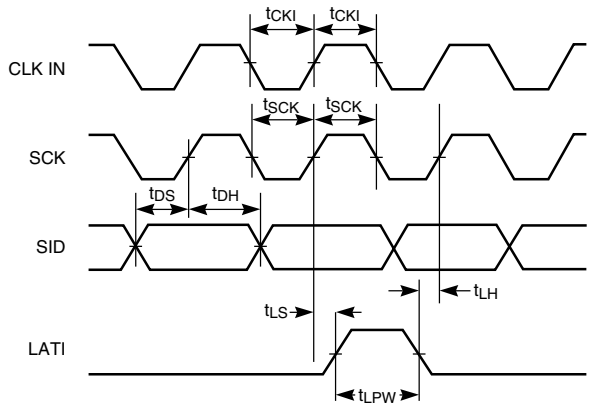
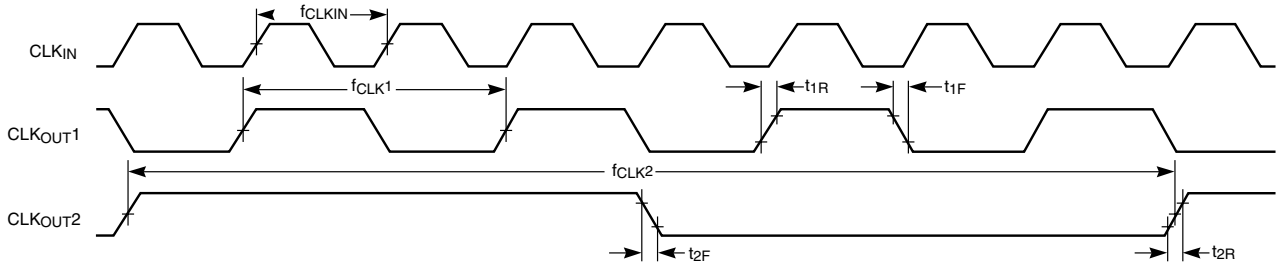


Figure 1. Serial Interface Timing.



f_{CLK} PARAMETERS REFERRED TO 1.4V MIDPOINT

Figure 2. Digital Clock Output Timing

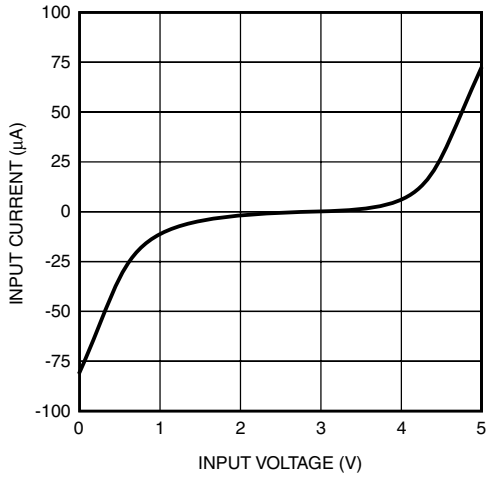


Figure 3. CLK IN Input Current vs. Input Voltage.

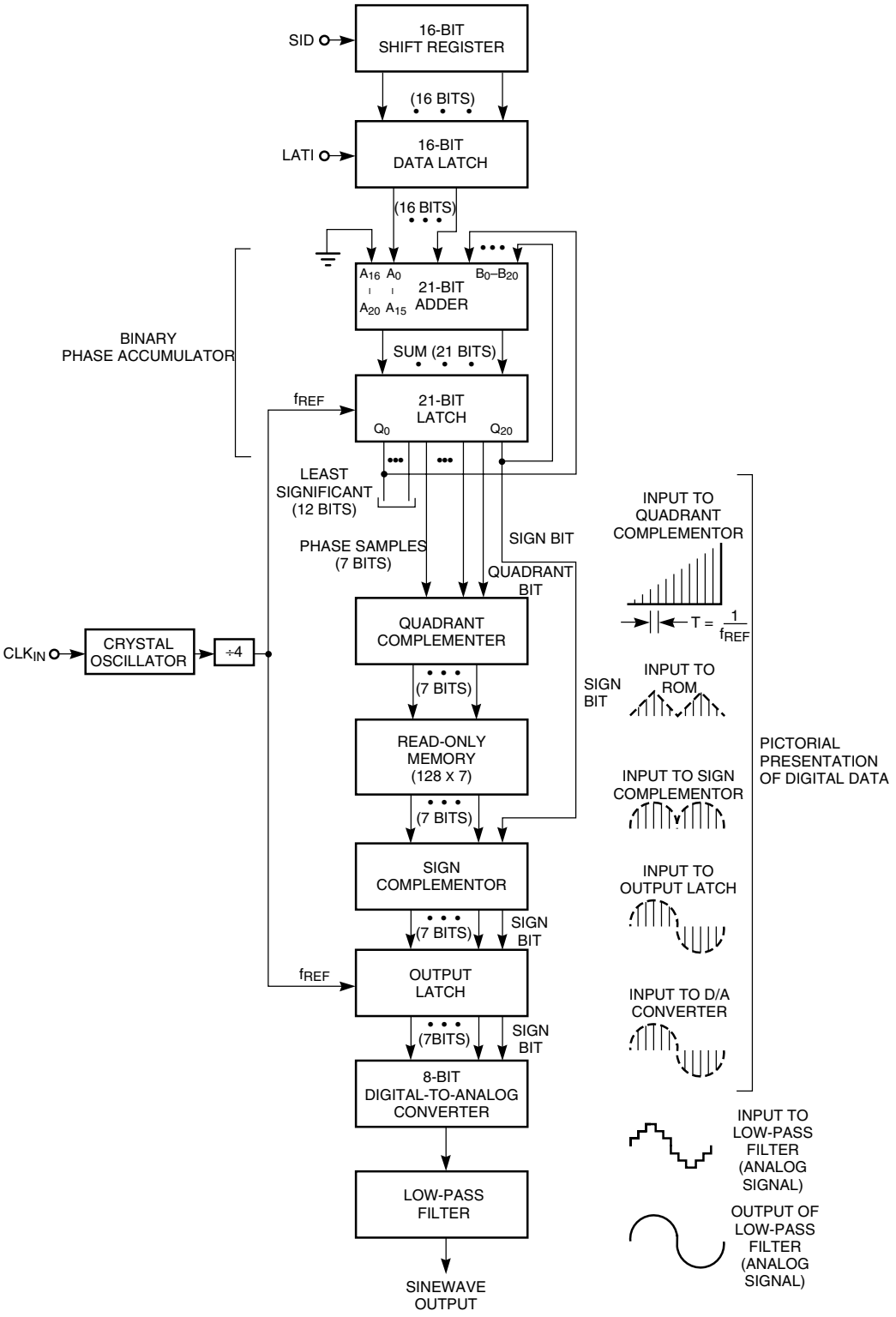


Figure 4. Detailed Block Diagram of the ML2036

Functional Description

The ML2036 is composed of a programmable frequency generator, a sine wave generator, a crystal oscillator, and a serial digital interface. The ML2036 frequency and sine wave generator functional block diagram is shown in Figure 4.

Programmable Frequency Generator

The programmable frequency generator produces a digital output whose frequency is determined by a 16-bit digital word.

The frequency generator is composed of a phase accumulator which is clocked at $f_{CLK\ IN}/4$. The value stored in the data latch is added to the phase accumulator every 4 cycles of CLK IN. The frequency of the analog output is equal to the rate at which the accumulator overflows and is given by the equation:

$$f_{OUT} = \frac{f_{CLKIN} X (D15 - D0)_{DEC}}{2^{23}} \quad (1)$$

The frequency resolution and the minimum frequency are the same and is given by the following equation:

$$\Delta f_{MIN} = \frac{f_{CLKIN}}{2^{23}} \quad (2)$$

When $f_{CLK\ IN}$ = 12.352MHz, Δf_{MIN} = 1.5Hz (±0.75Hz). Lower frequencies are obtained by using a lower input clock frequency.

Due to the phase quantization nature of the frequency generator, spurious tones can be present in the output range of –55dB relative to fundamental. The energy from these tones is included in the signal to noise + distortion specification. The frequency of these tones can be very close to the fundamental. Therefore, it is not practical to filter them out.

Sinewave Generator

The sinewave generator is composed of a sine look-up table, a DAC, and an output smoothing filter. The sine look-up table is addressed by the phase accumulator. The DAC is driven by the output of the look-up table and generates a staircase representation of a sine wave.

The output filter smoothes the analog output by removing the high frequency sampling components. The resultant voltage on V_{OUT} is a sinusoid with the second and third harmonic distortion components at least 45dB below the fundamental.

The ML2036 has a V_{REF} input that can be tied to V_{CC} or generated from an external voltage. With the GAIN input equal to a logic “1”, the sine wave peak-to-peak voltage is equal to $\pm V_{REF}$; with the GAIN equal to a logic “0”, the peak voltage is $\pm V_{REF}/2$. However, the overall output voltage swing is limited to no closer than 1.5V to either rail. This means that to avoid clipping, V_{REF} can only be tied to V_{CC} when GAIN is a logic “0”. The sinewave output is referenced to AGND.

The analog section is designed to operate over a range from DC to 50kHz. Due to slew rate limitations, the peak-to-peak output voltage must be limited to $V_{OUT(P-P)} \leq$ (125kV x Hz)/f_{OUT}. For example, an output at 50kHz must be limited to 2.5V_{P-P}. V_{OUT} can drive a 1kΩ, 100pF load and swing to within 1.5V of V_{CC} and V_{SS}, provided the slew rate limitations mentioned above are not exceeded.

The output offset voltage, V_{OS}, is a function of the peak-to-peak output voltage and is specified as:

$$V_{OS(MAX)} = \pm\left(\frac{2.5 + V_{OUT(P-P)}}{100}\right) \quad (3)$$

For example, if $V_{OUT(P-P)}$ = 2.5V:

$$V_{OS(MAX)} = \pm\left(\frac{2.5 + 2.5}{100}\right) = \pm 50mV$$

Crystal Oscillator

The crystal oscillator generates an accurate reference clock for the programmable frequency generator. The internal clock can be generated with a crystal or external clock.

If a crystal is used, it must be placed between CLK IN and DGND of the ML2036. An on-chip crystal oscillator will then generate the internal clock. No other external capacitors or components are required. The crystal should be a parallel-resonant type with a frequency between 3MHz to 12.4MHz. It should be placed physically as close as possible to the CLK IN and DGND.

An external clock can drive CLK IN directly if desired. The frequency of this clock can be anywhere between 0 and 12MHz.

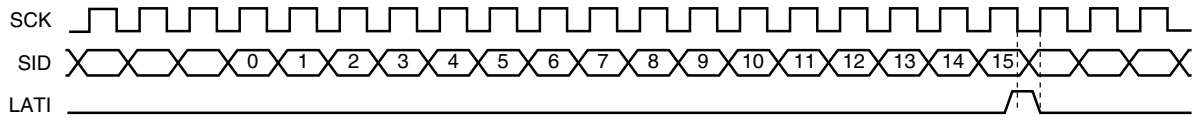


Figure 5. Serial Interface Timing.

The crystal must have the following characteristics:

1. Parallel resonant type
2. Frequency: 3MHz to 12.4MHz
3. Maximum equivalent series resistance of 15Ω at a drive levels of 1μW to 200μW, and 30Ω at drive levels of 10nW to 1μW
4. Typical load capacitance: 18pF
5. Maximum case capacitance: 7pF

The frequency of oscillation will be a function of the crystal parameters and PC board capacitance. Crystals that meet these requirements at 12.352000MHz are M-tron 3709-010 12.352 for 0°C to 70°C and 3709-020 12.352 for -40°C to 85°C operation.

The ML2036 has two clock outputs that can be used to drive other external devices. The CLK OUT 1 output is a buffered output from the oscillator divided by 2. The CLK OUT 2 output is a buffered output from the oscillator divided by 8.

Serial Digital Interface

The digital interface consists of a shift register and data latch. The serial 16-bit data word on SID is clocked into a 16-bit shift register on rising edges of the serial shift clock, SCK. The LSB should be shifted in first and the MSB last as shown in Figure 4. The data that has been shifted into the shift register is loaded into a 16-bit data latch on the falling edge of LATI. To insure that true data is loaded into the data latch from the shift register, LATI falling edge should occur when SCK is low, as shown in figure 1. LATI should be low while shifting data into the shift register to avoid inadvertently entering the power down mode. Note that all data is entered and latched on the edges, not levels, of SCK and LATI.

Inhibit and Power Down Modes

The ML2036 has an inhibit mode and a power down mode which are controlled by the three-level P_{DN}–INH input as described in Table 1. If a logic "1", (V_{I3}) is applied to the P_{DN}–INH pin, the power down mode is entered by entering all zeros in the shift register and applying a logic "1" to LATI and holding it high. A zero data detect circuit detects when all bits in the shift register are zeros. In this state, the power consumption is reduced to 11.5mW max, and V_{OUT} goes to 0V as shown in Figure 6 and appears as 10kΩ to AGND. CLK IN can be left active or removed during power down mode. Also, the ML2036 can be placed in the power down mode by applying a logic "0" to the P_{DN}–INH pin, regardless of the contents of the shift register and the state of LATI.

If V_{SS} to V_{SS} + 0.5V (V_{I2}) is applied to the P_{DN}–INH pin, the inhibit mode is entered by shifting all zeros into the shift register and applying a logic "1" to the LATI pin. Once the inhibit mode is entered V_{OUT} will complete the last half cycle of the sinewave and then be held at approximately V_{OS}, such that no voltage step occurs, as shown in Figure 6.

Power Supplies

The analog circuits in ML2036 are powered from V_{CC} to V_{SS} and are referenced to AGND. The digital circuits in the device are powered from V_{CC} to DGND. It is recommended that AGND and DGND be connected together close to the device, and have a good connection back to the power source.

It is recommended that the power supplies to the device should be bypassed by placing decoupling capacitors from V_{CC} to AGND and V_{SS} to AGND as physically close to the device as possible.

Table 1. Three Level P_{DN}-INH Functions.

P_{DN}-INH MODE	P_{DN}-INH PIN	DATA IN SHIFT REG.	LATI	SINE WAVE OUTPUT
P_{DN}(1)	V_{I1}, Logic "0"	X	X	V_{OUT} = 0V (10kΩ to AGND)
Inhibit	V_{I2}, Inhibit State Voltage, V_{SS} to V_{SS} + 0.5V	All 0's	Logic "1"	V_{OUT} goes to approximately V_{OS} at the next V_{OS} crossing (See Figure 6)
P_{DN}(1)	V_{I3}, Logic "1"	All 0's	Logic "1"	V_{OUT} = 0V (10kΩ to AGND)

Note:

1. In the power down mode, the oscillator, CLK OUT 1 and CLK OUT 2, shift register, and data latch are all functional.

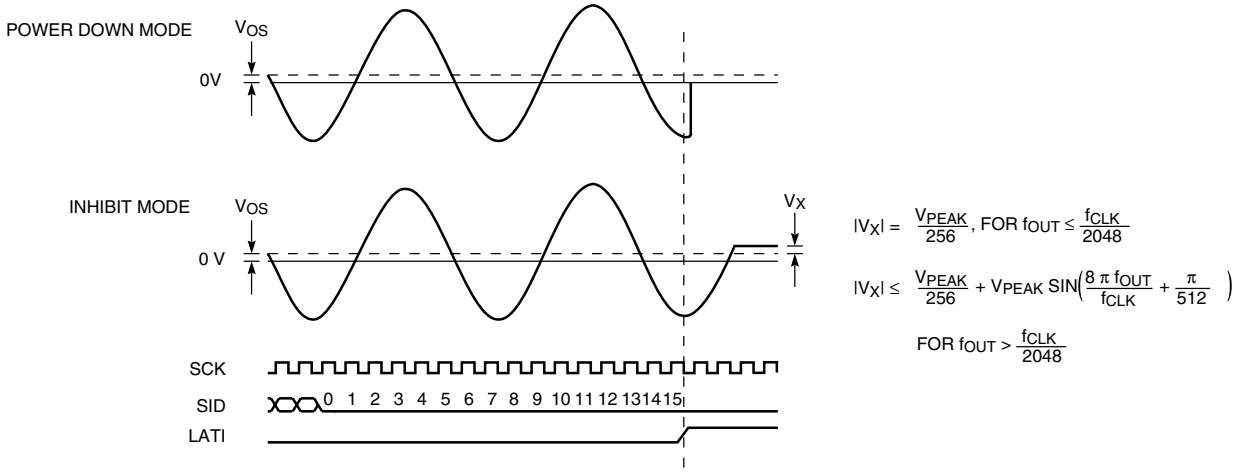


Figure 6. Power Down Mode Waveforms.

Typical Applications

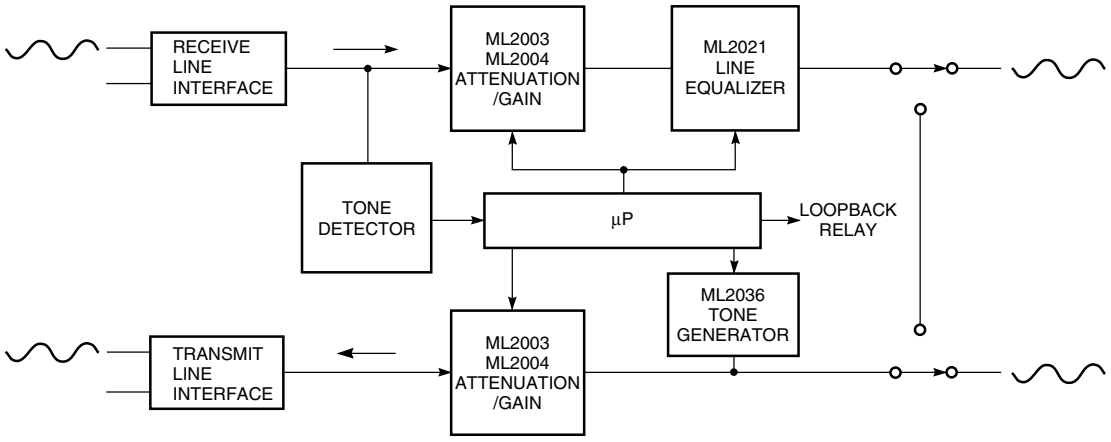


Figure 7. 4-Wire Termination Equipment.

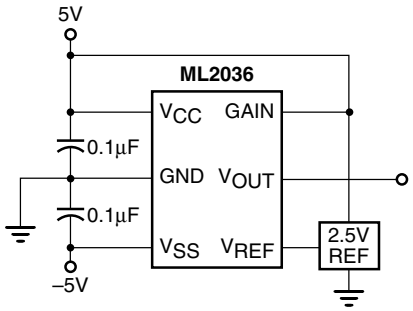
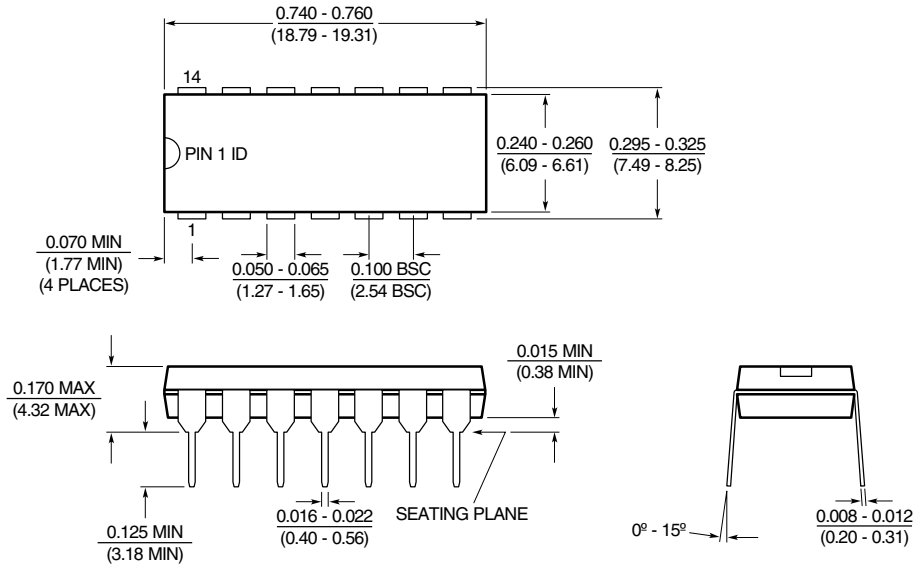


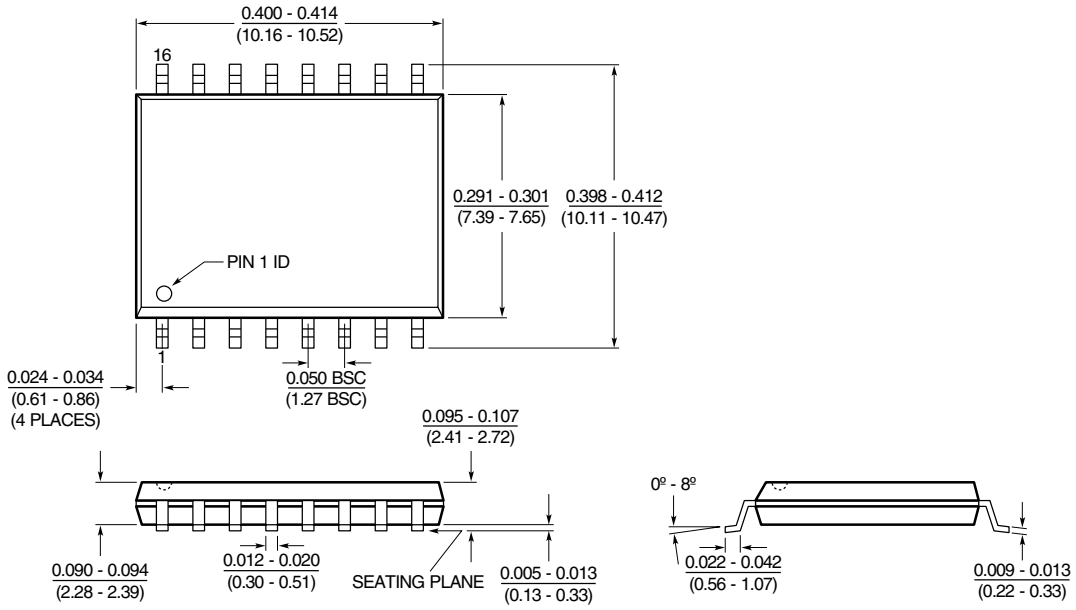
Figure 8. Sine Wave Generator with ± 2.5V$_{P-P}$.

Mechanical Dimensions Inches (Millimeters)

Package: P14
14-Pin PDIP



Package: S16W
16-Pin Wide SOIC



Ordering Information

Part Number	Temperature Range	Package
ML2036CP ML2036CS	0°C to 70°C 0°C to 70°C	14-Pin PDIP (P14) 16-Pin Wide SOIC (S16W)
ML2036IP	-40°C to 85°C	14-Pin PDIP (P14)

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